



Application Serial No. .... 09/920,979  
Filing Date ..... August 1, 2001  
Inventor..... H. Montgomery Manning  
Assignee ..... Micron Technology, Inc.  
Group Art Unit ..... unknown  
Examiner ..... undknow  
Attorney's Docket No. .... MI22-1698  
Title: Thin Film Transistors and Methods of Forming Thin Film Transistors

**RESPONSE TO AUGUST 29, 2001 NOTICE TO FILE CORRECTED  
APPLICATION PAPERS**

To: Box Non-Fee Amendment  
Assistant Commissioner for Patents  
Washington, D.C. 20231

From: Bernard Berman (Tel. 509-624-4276; Fax 509-838-3424)  
Wells, St. John, Roberts, Gregory & Matkin P.S.  
601 W. First Avenue, Suite 1300  
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Sir:

Responsive to the Notice To File Corrected Application Papers dated August 29, 2001, Applicant submits the following amended Abstract for the above-referenced application.

03CO



## UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS  
UNITED STATES PATENT AND TRADEMARK OFFICE  
WASHINGTON, D.C. 20231  
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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/920,979	08/01/2001	Monte Manning	MI22-1698

021567  
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CONFIRMATION NO. 6590

## FORMALITIES LETTER



\*OC000000006493128\*

Date Mailed: 08/29/2001

## NOTICE TO FILE CORRECTED APPLICATION PAPERS

*Filing Date Granted*

This application has been accorded an Application Number and Filing Date. The application, however, is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given **TWO MONTHS** from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a)

The required item(s) identified below must be timely submitted to avoid abandonment:

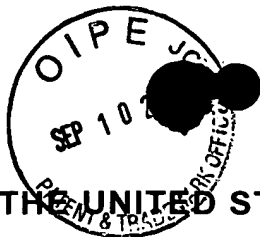
- An Abstract not to exceed 150 words in length, commencing on a separate sheet (37 CFR 1.72(b)).

*A copy of this notice **MUST** be returned with the reply.*

  
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Initial Patent Examination Division (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**  
**ACCOMPANYING RESPONSE TO AUGUST 29, 2001 NOTICE TO FILE**  
**CORRECTED APPLICATION PAPERS**

The Abstract of Disclosure has been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

~~A method~~ Methods of forming a thin film transistors, and transistors therefrom, are over a substrate is provided whereby at least one of the source region or the drain region is conductively doped while preventing conductivity doping of the channel region is prevented without any masking of the channel region occurring by any separate masking layer. ~~A method~~ Methods includes, a) providing a substrate having a conductive node, ~~to which electrical connection is to be made;~~ b) providing a first electrically insulative dielectric layer, over the substrate; ~~c) providing an electrically conductive~~ a gate layer over the first dielectric layer; ~~d) providing~~ and a second electrically insulative dielectric layer over the ~~electrically conductive~~ gate layer; ~~e) providing a contact opening through the first and second dielectric layers,~~ and the ~~electrically conductive gate layer,~~ and the first dielectric layer; the contact opening defining projecting sidewalls; f) providing a gate dielectric layer

within the contact opening laterally inward of the projecting sidewalls; g) providing a layer of semiconductive material over the second dielectric layer, and within the contact opening against the gate dielectric layer and in electrical communication with the node; the semiconductive material within the contact opening defining an elongated and outwardly extending a channel region; and the electrical conductance of which can be modulated by means of the adjacent electrically conductive gate and gate dielectric layers; and h) conductively doping the semiconductive material layer lying outwardly of the contact opening to form one of a source region or a drain region of a thin film transistor. Thin film transistor constructions are also disclosed.